REMARKS

Applicant requests reconsideration of their application in view of the foregoing amendments and the discussion that follows. The status of the claims as of this response is as follows: Claims 33-35 are now pending in the above-mentioned patent application and stand rejected. Claims 33-35 have been amended herein.

Applicant wishes to thank the Examiner for the courtesy of a telephonic discussion on July 10, 2003, in which the undersigned raised with the Examiner primarily matters of a formal nature.

The Amendment

The specification was amended to correct obvious typographical errors.

Claim 33 was amended to recite that each of the chips comprises an array of electronically addressable sites wherein each site is for electronically carrying out a chemical reaction and each site comprises an electrode. Support therefor is in the Specification, for example, original Claim 33 and page 21, lines 9-10. Claim 33 was also amended to recite that each of the individual chips comprises an array of electronically addressable sites and each site comprises an electrode. Support therefor is in the Specification, for example, original Claim 33 and page 21, lines 9-10.

Claim 34 was amended to indicate that each of the chips comprises an array of electronically addressable sites wherein each site is for electronically carrying out a part of a synthesis of oligonucleotides and each site comprises an electronic cell within the silicon substrate. Support therefor is in the Specification, for example, original Claim 33 and page 21, lines 9-10 and 17-18. Claim 34 further recites in step (b) that each of the chips comprises an array of electronically addressable sites and wherein each of the sites comprises an electronic cell within the silicon Support therefor is in the Specification, for example, original Claim 34 and page 21, substrate. lines 9-10 and 17-18.

Claim 35 was amended to recite that each of the chips comprises an array of electronically addressable sites wherein each site is for electronically carrying out a synthesis of an oligonucleotide of said oligonucleotides to form oligonucleotide arrays. Support therefor is in the Specification, for example, original Claim 35 and page 21, lines 9-10. Claim 35 also now recites severing the single silicon substrate into the individual chips wherein each of the chips comprises an array of

electronically addressable sites and wherein each of the sites comprises an electrode within the silicon substrate. Support therefor is in the Specification, for example, original Claim 35 and page 21, lines 9-10.

Rejection under 35 U.S.C. §112

Claim 35 was rejected under the second paragraph of the above code section as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Without in any way acquiescing in the position of the Examiner, Applicant submits that the above amendment obviates this ground of rejection.

Rejection under 35 U.S.C. §102

Claims 33-35 were rejected under paragraph (b) of the above code section as being anticipated by U.S. Patent No. 5,200,051 (Cozzette).

In order to maintain a rejection under 35 U.S.C. §102(b), the Examiner must first establish a *prima facie* case of anticipation. An invention is anticipated if each and every limitation of the claimed invention is disclosed in a single prior art reference. *In re Paulsen*, 30 F.3d 1475, 1478, 31 U.S.P.Q.2d 1671, 1673 (Fed. Cir. 1994). In the present situation Cozzette does not disclose each and every element of the claimed invention. The method of the invention of Claim 33 is directed to a method of fabricating a plurality of individual chips on a single silicon substrate. Each of the chips comprises an array of electronically addressable sites wherein each site provides for electronically carrying out a chemical reaction and each site comprises an electrode. The single silicon substrate is severed into the individual chips, each of which comprises an array of electronically addressable sites including an array of such electrodes.

Cozzette does not disclose or suggest the aforementioned method of the invention. Cozzette discloses dicing a wafer into individual biosensors for sensing a result of an analysis. Each individual biosensor is a single test site. On the other hand, in the present invention a single silicon substrate is severed into individual chips, each of which has an array of electronically addressable sites. Each of the sites provides for electronically carrying out a chemical reaction and each site includes an electrode. Accordingly, Cozzette does not teach each and every element of the present claim because Cozzette does not teach dicing a substrate into chips,

each having an array of electronically addressable sites including an array of electrodes.

The Examiner argues that the different areas and layers of the sensor of Cozzette read on the claimed array of electronically addressable sites and refers to Fig. 1 of the Cozzette patent. As can be seen from the disclosure of Cozzette (for example, column 16, lines 29-34), the various areas/layers of the chip of Fig. 1 refer to contact pads 1, signal line 2, passivation 3, silver/silver chloride reference electrode 4, metal catalytic indicator electrode 5, adhesion promoter 6, or localized adhesion promoter 7, coupling means 8 and ligand receptor layer 9. These layers constitute a single site and are not an array of electronically addressable sites each including an electrode. Therefore, Cozzette fails to disclose each and every element of the claimed invention of Claim 33. Thus, Cozzette does not anticipate Claim 33.

In addition, Cozzette indicates that the step of dicing the wafer to yield individual glucose sensors is a drastic step that is capable of effectively destroying all but the most robust thin-film structures that are present on the substrate wafer (column 40, lines 58-66). Of particular significance for his invention, continues Cozzette (column 40, line 67, to column 41, line 9), is the discovery that the dicing step can, in fact, be successfully performed on the embodiments of the glucose sensor "as described herein" without a deleterious effect on the selectivity, sensitivity and overall performance of the sensor.

Thus, the patentee found that the dicing method surprisingly worked for dicing a substrate into individual sensors. However, in the present invention the substrate is severed into individual chips, each bearing an array of electronically addressable sites. There is nothing in the teaching of Cozzette that would lead one skilled in the art to the expectation of success for severing a substrate into individual chips comprising such an array of sites. The array of sites for an individual chip of the present invention differs substantively from the individual sensor of Cozzette. The dicing process must not deleteriously affect the array of sites of the present chips. While Cozzette found surprisingly that the dicing worked for his individual sensors, the teaching does not provide the skilled artisan any confidence in the success of a method of dicing a substrate into chips with an array of addressable sites. Indeed, the teaching of Cozzette is for a special circumstance as is evident from Cozzette's disclosure referred to above.

At most, one could argue that it might have been obvious to try the method of Cozzette for severing a substrate into chips wherein each chip comprises an array of sites. However, obvious to try does not rise to the level of a bar against patentability. Certainly, obvious to try does not rise to the level of anticipation.

Claim 34 is not anticipated or suggested by the disclosure of Cozzette. The method of the invention of Claim 34 is directed to a method of fabricating a plurality of individual chips on a single silicon substrate. Each of the chips comprises an array of electronically addressable sites wherein each site provides for electronically carrying out a chemical reaction and each site comprises a cell within the silicon substrate. The single silicon substrate is severed into the individual chips, each of which comprises an array of electronically addressable sites and each of which comprises an electronic cell within the silicon substrate. Cozzette does not disclose or suggest such a method.

The invention of Claim 35 is directed to a method of fabricating a plurality of individual chips for conducting a synthesis of oligonucleotides in the form of oligonucleotide arrays. A plurality of the chips is prepared on a single silicon substrate. Each of the chips has an array of electronically addressable sites for electronically carrying out a part of the synthesis of the oligonucleotides in the form of oligonucleotide arrays. The single silicon substrate is severed into the individual chips wherein each of the chips comprises an array of electronically addressable sites and wherein each of the sites comprises an electrode within the silicon substrate.

Cozzette does not disclose or suggest the aforementioned method of the present invention. Cozzette discloses dicing a wafer into individual biosensors for sensing a result of an analysis. On the other hand, in the present invention a single silicon substrate is severed into individual chips, each of which has an array of electronically addressable sites and each of the sites comprises an electrode within the silicon substrate. Clearly, the array of electronically addressable sites of a chip of Claim 35 is substantially different from the chip of Cozzette with an individual sensor.

As mentioned above, the patentee found that the dicing method surprisingly worked for dicing a substrate into individual sensors. However, there is nothing in the teaching of Cozzette that would lead one skilled in the art to the expectation of success for severing a substrate into individual chips comprising such an array of sites. The dicing process must not deleteriously affect the array of sites of the

present chips. While Cozzette surprisingly found that the dicing worked for dicing into individual sensors, the teaching has little applicability to dicing a substrate into chips with an array of addressable sites.

Conclusion

Claims 33-35 satisfy the requirements of 35 U.S.C. 102 and 112. Allowance of the above-identified patent application, it is submitted, is in order.

Respectfully submitted,

Theodore J Leitereg
Attorney for Applicant
Reg. No. 28,319

Agilent Technologies, Inc.
Legal Department, M/S DL429
Intellectual Property Administration
P.O. Box 7599
Loveland, CO 80537-0599
(650) 485-3864